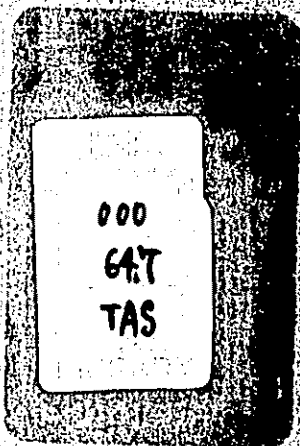


**FULL SOLID-STATE 100 W FM  
REBROADCASTING TRANSMITTER**



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## FULL SOLID-STATE 100 W FM REBROADCASTING TRANSMITTER

In conventional FM rebroadcasting transmitters, solid-state elements were used for output power, up to the 10 W stage, and forced air-cooled-vacuum tubes, such as 4F64, were used for output power up to 100 W stages.

Further, in order to improve the reliability and maintainability, vacuum tubes were replaced with solid-state elements, thus the full solid-state 100 W transmitters (50 VV-71 type) have been developed.

### 1. Composition and Block Diagram of FM Rebroadcasting Transmitter

The composition and block diagram of the full solid-state FM rebroadcasting transmitter is shown in Fig. 1 and 2, respectively.

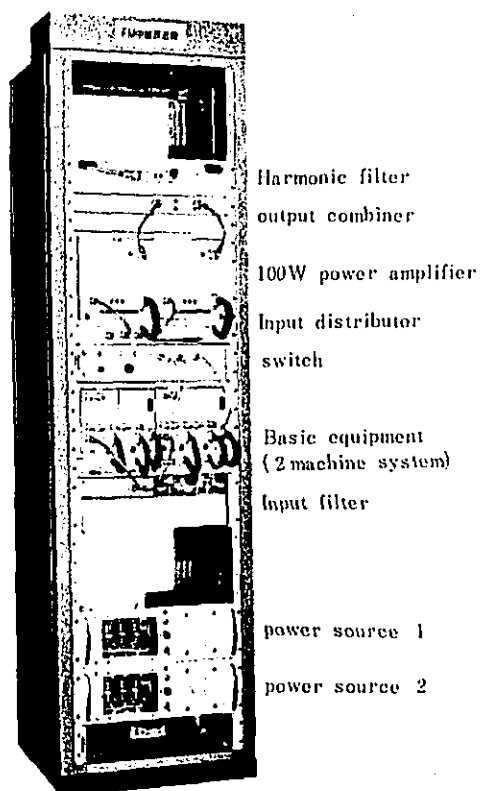


Fig. 1 Composition of Full Solid-State 100 W FM Rebroadcasting Transmitter

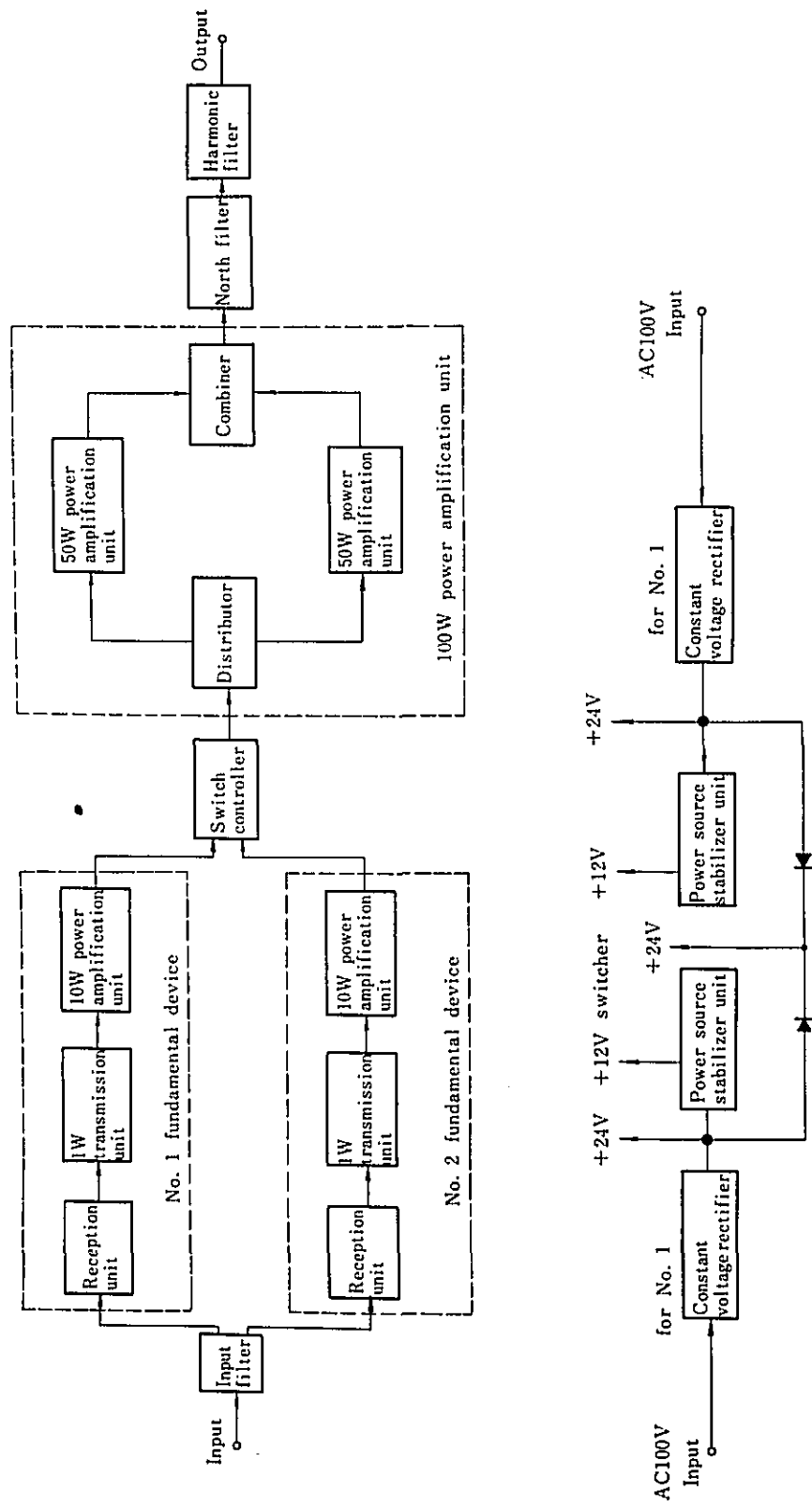


Fig. 2 Block Diagram of Full Solid-State 100 W FM Rebroadcasting Transmitter

There are two fundamental devices, No.1 and No.2, consisting of a receiver unit, 1 W transmitter unit and a 10 W power amplification unit. The 10 W output power of each fundamental device can be selected and switched over by a switching control unit, and connected to the solid-state 100 W power amplification unit.

The output power of 10 W device is divided by a distributor into two 5 W outputs and applied to the 50 W power amplification unit. The two 50 W outputs of the two power amplification units are combined with a combiner to a power of 100 W, and then fed to the antenna through a notch-filter and harmonic filter.

The power supply required for each fundamental device is 12 V, 1A and 24V, 7.5A. The 12 V power source is obtained by stabilizing the 24 V output power source.

The 24 V power source for the switcher unit is obtained by combining the power source of devices, No. 1 and No. 2, in common.

## 2. . Solid-State 100 W Power Amplification Unit

### 2.1 Outline and Principles of Design

The external dimension of the 50 W power amplification unit is 214 (H) x 290 (W) x 220 (D) and two of the units are set on a rack shelf width of 250 mm.

Table 1 indicates the ratings and principle performances.

The principle of design is same as the previous stage 10 W power amplification unit, in consideration of the following items.

- (1) Can be replaced with the conventional power amplifiers.
- (2) By parallel operation of the two 50 W power amplification units, the reliability will be improved for reducing failure of transmitter breakdown.
- (3) To ensure the centralized control of the ancillary materials, the amplification circuit is of wide-band

characteristic, covering frequency range of 76 - 90 MHz and can be used at an arbitrary frequency by exchanging the circulator.

- (4) For power distribution combiners, the LC lumped constant  $\lambda/4$  cable type and 3 dB coupler type, etc. are available, but in this case, the former type is adopted.

## 2.2 Block Diagram and Level of Each Portion

Fig. 3 indicates a schematic diagram of the whole 100 W power amplification system and, the operation level of each portion.

Since there is a total loss of 0.9 dB with regard to insertion loss of notch filter, harmonic filter and directional coupler, a 123 W output is needed to obtain a rated output power of 100 W.

Table 1. Rating and Major Performances of 100 W Power Amplifier

Item		Ratings and performances
Input	Frequency, impedance, level	76-90 MHz 50 $\Omega$ , VSWR less than 1.3 10 W, $\pm 1$ dB adjustable
Output	Frequency, impedance, level	Specified frequency of 76- 90 MHz 50 $\Omega$ , matches with load of VSWR less than 1.3 Adjustable up to 100 W + 1 dB (reduceable to 30 W as for applicable output)
Frequency band characteristics		Frequency deviation, excluding circulator for 76 - 90 MHz is $\pm 0.5$ dB
Spurious		Against fundamental wave; Second harmonics           less than -30 dB Third harmonics           less than -40 dB Fourth harmonics           less than -50 dB Fifth harmonics           less than -60 dB Other than harmonics       less than -65 dB
Excessive input		Withstand up to rating + 3 dB
Stability		Withstand input/output opening



Item	Ratings and performances
Transistor loss	Conforming to the specification of the NHK semi-conductor handbook
Power source	DC + 24 V less than 12A (at output rating + 1 dB).

If we presume a loss of 0.6 dB with respect to the output power combiner and, 50 W power amplification unit combiner and circulator, an output of 37 W is required per transistor. To fulfill this condition two 2SC1022 transistors were adopted and connected in parallel.

Table 2 indicates the major ratings and performances of transistor 2SC1022. An input of 10 W will be available owing to the existing equipment, but as there is sufficient gain, a 3 dB ATT is inserted.

A wide-band transformer is applied to the input/output circuit of the transistor amplifier. Thus the circuit configuration has become simplified and compact and, wide-band operation has become available. As the coupling impedance is kept low, induction between circuit elements is reduced and therefore, it has become stable against oscillation. Shortcomings are difficulties of the selection of an arbitrary conversion ratio, probability of generation of spurious due to wide-band and, occasional low-frequency oscillation due to the frequency extension to the lower frequency range. The input impedance of the final stage transistor is rather low, accurate data is not available, but it is about 1 ohm. As there is a considerable fluctuation in this value, difficulty exists in matching adjustment.

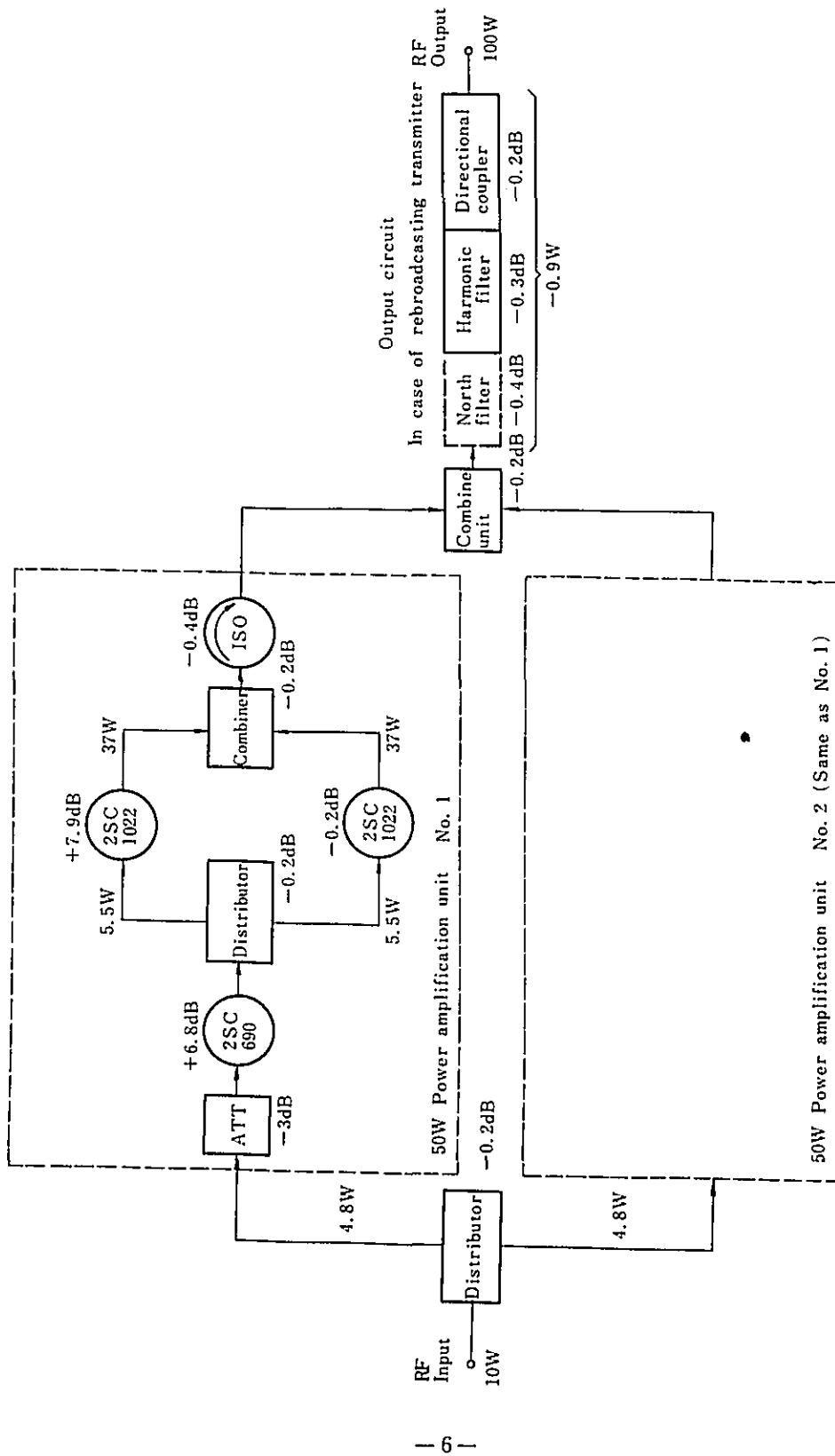


Fig. 3. Overall System of 100 W Power Amplifier

The adoption of wide-band system for circulators was envisaged but in consideration of the insertion loss in the VHF band, the spacing and cost, it was determined to use a circulator exclusive for each frequency. Fig. 4 indicates the performances of the circulator, but practically, a single circulator can cover frequencies within a range of  $\pm 1$  MHz.

Table 2. Major Ratings and Performances of 2SC1022

Item	Symbol	Ratings
Voltage between collector and base	Vcbo	60 V
Voltage between emitter and base	Vebo	5 V
Voltage between collector and emitter	Vceo	40 V
Collector current	Ic	6 A
Collector loss	Pc	60 W
Junction temperature	Tj	+175°C
Preservation temperature	Tsto	-65 ~ 175°C
Thermal resistance	Rth- C	2.5°C/W
Tightening torque	—	30 kg-cm
Output power	Minimum 40 W	Measuring condition: Eb = 28V, f = 90 MHz, Pi = 5 W
Efficiency	Minimum 60 %	

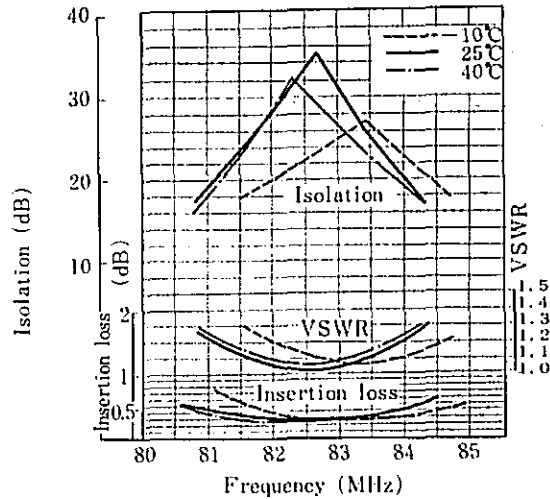


Fig4. Performance of circulator

### 2.3 Final Stage Transistor Output Circuit

Fig. 5 indicates the final stage 2SC1022 transistor circuit and impedance of each portion and wave-form of high-frequency voltage. The operating condition of the circuit is influenced by the second harmonics because of wide-band amplification, as seen in the collector wave-form. By analyzing this wave-form, it can be realized that the Fourier components of the sinusoidal partial wave, i.e. the fundamental wave and the second harmonic contribute to suppress the negative side-peak, thus resulting in a phase relationship close to a square waveform in combining a waveform.

It is difficult to obtain an accurate power operation performance of a high frequency transistor, but approximate values are presented for reference. From the level of the block diagram, presuming that  $P_0 = 37 \text{ W}$ ,  $E_b = 24 \text{ V}$ ,  $\theta_c = 90^\circ$ ,  $\xi_v = 0.95$  for per transistor, the following values are obtained.

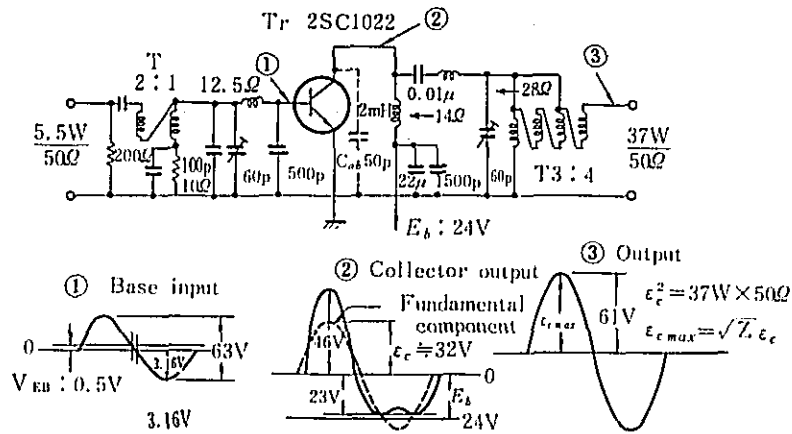


Fig. 5 Final Stage Circuit and High Frequency Wave-form of Each Part

Collector fundamental wave voltage	$\epsilon_c = \xi_v \cdot E_b = 23 \text{ V}$
Collector fundamental wave current	$\vartheta_c = 2P_0 / \epsilon_c = 3.21 \text{ A}$
Collector current peak value	$i_{c \text{ max}} = 2 \vartheta_c = 6.42 \text{ A}$
Collector DC current	$I_c = i_{c \text{ max}} / \pi = 2.05 \text{ A}$
Collector DC input	$P_{dc} = E_b \cdot I_c = 49.4 \text{ W}$
Collector efficiency	$\eta_c = P_0 / P_{dc} = 75\%$
Transistor overall efficiency	$\eta_t = P_0 / (P_{dc} + P_i) = 68\%$
Load impedance	$R_L = \epsilon_c / \vartheta_c = 7.15$

The fundamental wave component  $\epsilon_c$  from the actual collector voltage wave-form is considered to be approx. 32V and, from this,  $P_0 = \epsilon_c^2 / 2R_L$  and  $R_L = 13.8 \Omega$  are obtained. This value is approximately 2 times of the approx. calculated  $R_L$  (7.15  $\Omega$ ), and the actual matching is taken at this value.

Fig. 6 indicates the frequency characteristics of the 50 W power amplification unit. Almost flat output is obtained throughout a range of 76 - 90 MHz.

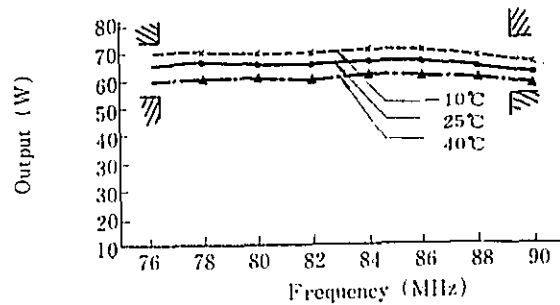


Fig. 6 Frequency Characteristics of 50 W Power Amplification Unit

#### 2.4 Heat Dissipation Measures

The reliability of the transistor circuit largely depends upon the junction temperature of the operation condition. Therefore, it is quite important to lower the junction temperature to improve the reliability, but in case of large output transistors, the reliability is determined almost exclusively by the thermal resistance and the operational efficiency of the transistor itself, so the efficiency will become the most important factor.

In our case, design is based on the NHK's semi-conductor application standard " $T_j$  should be less than  $110^\circ\text{C}$  at  $T_a = 45^\circ\text{C}$ ". Heat dissipation is natural cooling by fins. The necessary resistance of the heat dissipating fin is calculated. Since  $P_o = 37\text{ W}$  for the final stage 2SC1022, the following values are obtained on the presumption that the overall efficiency  $\eta_o = P_o / P_i + E_b \cdot I_c = 66\%$ .

$$P_i + E_b \cdot I_c = 56\text{ W}$$

$$\therefore \text{Total loss} \quad P_{\text{Loss}} = 56 - 37 = 19\text{ W}$$

$$\text{Total thermal resistance} \quad R_{\text{th}} = T_j - T_a / P_{\text{Loss}} = 3.41^\circ\text{C/W}$$

$$T_r \text{ thermal resistance} \quad R_{\text{th-c}} = 2.5^\circ\text{C/W}$$

Necessary thermal resistance of the heat dissipation fins  $R_F$

is obtained as follows, based on the presumption that the contact resistance  $\theta = 0.2^\circ\text{C}/\text{W}$ .

$$R_F = 3.41 - 2.5 - 0.2 = 0.71^\circ\text{C}/\text{W}$$

Similar calculation is made with regard to 2SC690, and it will be realized that the total loss will be 6 W and thermal resistance will be  $5.6^\circ\text{C}/\text{W}$ .

Based on the above results, two 2SC1022 and one 2SC690 are installed on one fin, so that the fin must dissipate a total loss of  $19\text{ W} \times 2 + 6\text{ W} = 44\text{ W}$ . The thermal dissipating circuit for that purpose is obtained as shown in Fig. 7, so that the overall thermal resistance of the fin will be less than the following value.

$$R_F = 13.7/44 = 0.31^\circ\text{C}/\text{W}$$

Thus the fin as shown in Fig. 8 is applied for the installation of transistors. The thermal resistance of the fin is  $0.25^\circ\text{C}/\text{W}$  which satisfies the designed value for one fin. However, a supplementary fin has been attached on the back surface of the unit in consideration of the degradation of environmental conditions, etc., for back up purpose.

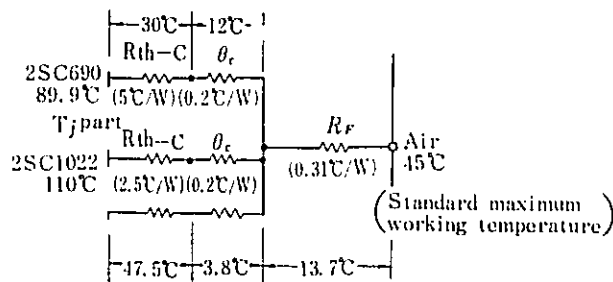


Fig. 7 Thermal Circuit of Transistor

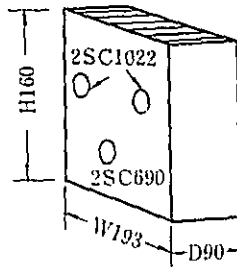


Fig. 8 Heat Dissipation Fin

Table 3. Operating Performances of Transistor

Table 3. Operating Performances of Transistor

Transistor	Items	DC voltage E <sub>b</sub> (v)	DC collector current I <sub>c</sub> (A)	DC input P <sub>dc</sub> (W)	RF input P <sub>i</sub> (W)	RF output P <sub>o</sub> (W)	Thermal resistance R <sub>th-c</sub> (°C/W)	Case temperature (T <sub>a</sub> =25°C) T <sub>c</sub> (°C)	Junction temperature T <sub>j</sub>	
									T <sub>a</sub> =25°C	T <sub>a</sub> =45°C
T <sub>r1</sub>	2SC690	23	0.72	16.6	2.4	12	5	40	75	95
T <sub>r2</sub>	2SC1022	24	2.15	52	5	38	2.5	41	86.5	108.5
T <sub>r3</sub>	2SC1022	24	2.1	50.6	5	39	2.5	41	82.5	102.5

$$T_j = T_c + ((E_b \times I_c) + P_i - P_o) \times R_{th-c} \quad T_a : \text{Ambient temperature}$$

As mentioned above, an operation-data was obtained as given in Table 3 and, this satisfied the junction temperature of less than 110°C at an ambient target temperature of 45°C. Further, with respect to the final stage operation of T<sub>r2</sub> of low efficiency, a performances close to the designed values were obtained; namely  $\eta_1 = 38 / (52 + 5) = 66.7\%$ , collector efficiency  $\eta_c = 73\%$ ,  $P_{Loss} = 57 - 38 = 19$  W when E<sub>b</sub> = 24 V, P<sub>o</sub> = 38 W, P<sub>i</sub> = 5 W and I<sub>c</sub> = 2.15 A.



### 3. Adjustment and Maintenance

With regard to the fundamental devices, refer to the aforementioned IC FM rebroadcasting transmitters. The following will be dealing with the 100 W stage.

As the operation of 100 W unit is in the level relationship as described above, confirmation should be made on whether the combined output is equal to the summation of both units.

Since a circulator is inserted in the 50 W output, open circuit of the output terminals will not cause damage to the final stage, but attention should be paid to open-circuit.

The rated output is obtainable from the power amplification unit without any adjustment. In case a small fluctuation occurs, it can be adjusted by power adjustment. In case of large fluctuation appears, inspection is necessary because the unit may be in trouble.

In case the frequency is to be changed, the circulator must be replaced.

